Rishi Bala

Millburn, NJ • rishibala@utexas.edu • (973) 419-3663 • linkedin.com/in/rishi-bala25/ • github.com/rbala25

Education

The University of Texas at Austin, Austin, Texas — May 2028

- GPA: 3.97/4, BS: Electrical and Computer Engineering Honors, BBA: Canfield Business Honors, ACT: 36/36
- **Relevant Coursework**: Computer Architecture, Digital Logic Design, Software Design, Circuit Theory, Embedded Systems

Experience

IPC Systems | New York, New York — May 2026 – Present

Embedded Firmware Intern

- Replaced polling-based turret screenshot delivery with live streaming by benchmarking VNC and WebRTC pipelines on embedded Linux BSP hardware, measuring end-to-end frame latency to drive a production protocol decision for financial trading floors.
- Instrumented the embedded turret diagnostics pipeline, pulling live performance metrics from all trading floor endpoints.
- Extended the Rust/Tauri hardware interface with WAMP command surfaces, bridging the turret BSP to a desktop viewer.
- Worked with senior engineers to design the hardware-software stack covering BSP daemons in C/C++ with GStreamer and Wayland, an encrypted transport layer, and the Rust/Tauri viewer, tracing the full signal path from turret BSP to trading floor desktop.

Longhorn Racing – Electric | Austin, Texas — August 2025 – Present

Controls System Lead (Competing in the Formula SAE International Competition)

- Led the controls electronics subteam, owning board-level architecture and requirements documentation across the vehicle.
- Drove electronics architecture across multiple boards (VCU, TSM, PDU), authoring board requirements and the electronics FMEA.
- Wrote STM32 control and telemetry firmware across boards with deterministic CAN, multi-sensor interfacing, and FreeRTOS.
- Designed an automotive-grade wiring harness: connector selection, crimping, CAN routing, and full-vehicle integration.
- Designed shutdown interlocks, fault detection, and watchdog coverage across every board and subsystem in the vehicle.
- Coordinated integration with the mechanical and HV subteams, logging 250+ validation miles ahead of the FSAE competition.

Projects | www.rishibala.com

FPGA-Based CME Market Making Engine — April 2026 – June 2026

GitHub Repository

- Designed a fully pipelined, CPU-free market maker in SystemVerilog on a Xilinx Artix-7 with a complete Ethernet/TCP/IP network stack, CME MDP 3.0 market data, and iLink 3 FIXP order entry across 25 RTL modules; sub-µs logic-pipeline tick-to-order latency.
- Implemented a CME MDP 3.0 market data pipeline decoding SBE-encoded UDP multicast packets across incremental and snapshot feeds, with a 10-level order book in RTL featuring gap detection and automatic snapshot-based sequence recovery.
- Built a quoting engine computing VWAP mid-price via a pipelined 64-bit integer divider, adjusting bid/ask quotes for inventory skew and an exponentially-decaying Order Flow Imbalance (OFI) signal derived from real-time aggressor trade data.
- Wrote self-checking testbenches for all 25 modules and brought the full design up on an Arty A7 with a DP83848 MII PHY.

Vehicle Control Unit (VCU) — July 2026 – Present

Hardware Repository | *Software Repository*

- Designed and built the VCU end to end in KiCad around an STM32G474, owning both the schematic and the firmware running on it.
- Architected the analog front end (TVS, dividers, RC filtering, op-amp buffers) sizing every channel for STM32 ADC integrity.
- Wrote FreeRTOS firmware driving the ready-to-drive state machine, sensor acquisition with plausibility, and CAN telemetry.
- Arbitrated torque across APPS, regen, and torque-vectoring inputs, resolving driver intent against grip and thermal limits.
- Built hardware-only safety logic (BSPD, shutdown sequencing, plausibility checks) enforced independently of firmware; sensed both ends of the 24V shutdown loop so firmware can localize whether it opened upstream or at the VCU's own relay.

FPGA Pattern-Matching Accelerator with Cache Hierarchy — June 2026 – August 2026

GitHub Repository

- Built an FPGA Aho-Corasick multi-pattern matching accelerator in SystemVerilog on an Arty A7 for streaming byte inputs.
- Placed the oversized transition table behind a latency-modeled memory, fronted by an SRAM cache exploiting state locality.
- Swept LRU, FIFO, and random replacement against a novel static placement pinning high-traffic automaton rows in BRAM; static hit 34 vs. 26 for FIFO/random (31%, zero warmup), with no runtime overhead where access is statically fixed.
- Verified all four replacement policies in UVM with 0 errors and 0 fatals across a 47-byte multi-pattern stream; wrote a Python reference model to generate Aho-Corasick automata and transition tables as ground truth for automated UVM checking.

Additional Information and Skills

Technical Skills: SystemVerilog, Verilog, FPGA, Vivado, UVM, C/C++, Rust, RTOS, STM32, CAN, PCB Design, AXI4-Lite, CDC
Honors: University Honors 2x, VEX Robotics World Finalist, World Division Champion, National Merit Commended Scholar
Interests: Pickleball, Motorsport, Drums, Jazz, Tennis, Go-Karting
Work Eligibility: Eligible to work in the U.S. with no restrictions